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Published in:
4th International Conference on Power Engineering, Energy and Electrical Drives

DOI:
10.1109/PowerEng.2013.6635752

Publication date:
2013

Document Version
Author accepted manuscript

Predictive Voltage Control of Phase-Controlled Series-Parallel Resonant Converter

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***Abstract*—This paper proposes a predictive output voltage controller for the phase-controlled series-parallel resonant converter. The objective of this controller is to enhance closed loop system robustness and dynamic performance compared to conventional PI control. First, the converter non-linear large signal behavior is linearized using a state feedback based scheme. Consequently, the converter preserves its large signal characteristics while modeled as a linear system. A reduced order model is then used for the detailed design of the proposed predictive controller. Stability analysis and controller gains selection are addressed. Finally, simulation and experimental results are demonstrated to validate the improved system performance in contrast with PI control.**

***Keywords*-Phase control, predictive control, robustness, series-parallel resonant converter (SPRC).**

I. INTRODUCTION

Resonant converters are an alternative to hard-switched PWM converters in dc power supply applications. This is due to their soft switching characteristics; hereby boosting switching frequency and reducing converter footprint. This feature has been very attractive in modular multi-cell dc/dc converters catering for fault tolerant high power dc supplies.

The series-parallel resonant converter (SPRC) has been one of the main resonant converter topologies subject to rigorous research in the past [1-6]. It can operate over a large input voltage range and a large load range (no load to full load) while maintaining high efficiency. Several linear and non-linear control techniques have been reported for SPRC [7-10]. Among them, non-linear techniques have received particular attention due to the improvement of the transient response, robustness, and stable behaviour against load and input voltage variations. However, non-linear control laws are usually complex, which makes practical control implementation difficult. Fast, simple and robust sliding-mode controllers were proposed for a zero current switching (ZCS) SPRC operating with quantum-mode control [11]. A sliding mode controller design approach was applied in [12] to a zero voltage switching (ZVS) SPRC using the self-sustained phase shift modulation technique introduced in [13]. The latter technique, although providing ZVS for the whole load range with good output voltage regulation, varies the switching frequency to obtain this goal. Practically, varying switching frequency is undesirable due to EMI problems. For this reason, this paper focuses on the fixed frequency phase control technique of SPRC [14-19].

Conventional PI control design methods based on small signal modelling of the converter depend on linearizing converter large signal model around an equilibrium point. Although eliminating error in output voltage, dynamic response is only satisfactory in a close neighbourhood to the steady state operating point selected [20]. In addition, under PI control, high proportional gain is necessary to achieve high system robustness, disturbance rejection capability and dynamic performance. This results in lower closed loop stability margins and oscillatory system behaviour. To achieve better robustness and dynamic performance with reasonable closed loop stability, this paper proposes a predictive output voltage controller for the phase-controlled SPRC based on a two-loop structure. The derivation of the controller structure is based on linearizing the converter large signal model using a state feedback scheme where output filter inductor current is sensed and used for linearization. This facilitates the controller design procedure.

The paper is organised as follows. In section two, the converter model and state feedback linearization scheme are outlined [21]. Predictive controller design is addressed in section three. Stability analysis is given in section four and accordingly controller gains are selected. Finally, simulation and experimental results are used to validate controller performance in section five.

II. SPRC LINEARIZED LARGE SIGNAL MODEL

Fig. 1 shows the circuit diagram for a typical SPRC. Two stages of conversion exist; dc/ac (inversion) and ac/dc (rectification). Hence, two main subsystems exist; the ac sub-system (resonant tank and transformer) and the dc sub-system (output filter), as illustrated in Fig. 2. Each sub-system has its own state variables; therefore, both ac and dc state variables exist.

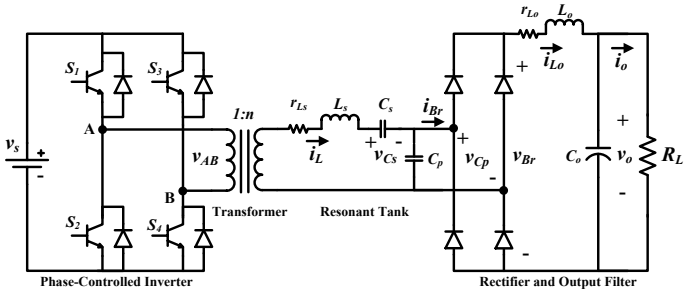


Fig. 1. Circuit diagram for the SPRC.

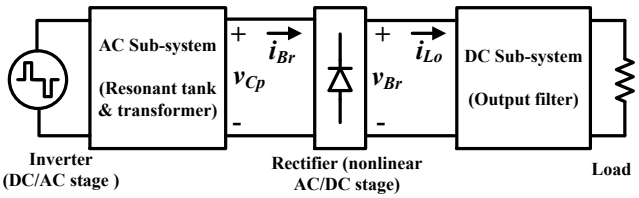


Fig. 2. SPRC conversion stages and subsystems.

In order to combine both types of signals into one model, it is essential to transform the ac state variables to equivalent dc quantities. This is achieved with the multiple frequency modeling technique which converts the ac state variables to *d-q* quantities using the harmonic balance theory [22]. The resulting dc state variables from the resonant tank are combined with the natural dc state variables of the output filter side (modeled with conventional average state-space modeling) using a linearization scheme to overcome the non-linearity imposed by the rectifier. The result is an aggregate large signal linear model for the complete converter.

A. Ac sub-system modeling

Fig. 3(a) illustrates the ac subsystem equivalent circuit, where v_{AB}` is the inverter output voltage referred to secondary and r_T with L_T represent the total equivalent series impedance taking into account transformer copper resistance and leakage inductance respectively. Applying harmonic balance theory and assuming fundamental ac components only with angular frequency ω_s, model can be represented by

$$\dot{\vec{x}}_1(t) = A_1\vec{x}_1(t) + B_1\vec{u}(t) \tag{1}$$

where

$$\vec{x}_1(t) = [i_{Ld}\ i_{Lq}\ v_{Csd}\ v_{Csq}\ v_{Cpd}\ v_{Cpq}]^T,\ \vec{u}_1(t) = [v_{ABd}`\ v_{ABq}`\ i_{Brd}\ i_{Brq}]^T,$$

$$A_1 = \begin{bmatrix} -\frac{r_T}{L_T} & \omega_s & -\frac{1}{L_T} & 0 & -\frac{1}{L_T} & 0 \\ -\omega_s & -\frac{r_T}{L_T} & 0 & -\frac{1}{L_T} & 0 & -\frac{1}{L_T} \\ \frac{1}{C_s} & 0 & 0 & \omega_s & 0 & 0 \\ 0 & \frac{1}{C_s} & -\omega_s & 0 & 0 & 0 \\ \frac{1}{C_p} & 0 & 0 & 0 & 0 & \omega_s \\ 0 & \frac{1}{C_p} & 0 & 0 & -\omega_s & 0 \end{bmatrix} \quad B_1 = \begin{bmatrix} \frac{1}{L_T} & 0 & 0 & 0 \\ 0 & \frac{1}{L_T} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_p} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_p} \end{bmatrix}$$

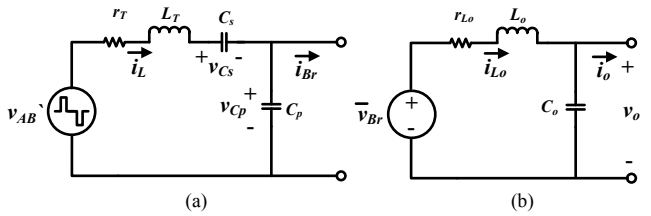


Fig.3. Equivalent circuit diagram for (a) ac sub-system, and (b) dc sub-system.

B. Dc sub-system modeling

Fig. 3(b) shows the equivalent circuit diagram for the SPRC dc sub-system. Note that $\overline{v}_{Br}$ is the average rectifier output voltage v_{Br}. Energy is transferred at dc frequency, so the dominant component for modeling and analysis is the dc (average) value. For this reason, average state-space modeling is valid for modeling the dc sub-system

$$\dot{\vec{x}}_2(t) = A_2\vec{x}_2(t) + B_2\vec{u}(t) \tag{2}$$

where

$$\vec{x}_2(t) = [i_{Lo}\ v_o]^T,\ \vec{u}_2(t) = [v_{Br}\ i_o]^T,\ A_2 = \begin{bmatrix} -\frac{r_{Lo}}{L_o} & -\frac{1}{L_o} \\ \frac{1}{C_o} & 0 \end{bmatrix},\ B_2 = \begin{bmatrix} \frac{1}{L_o} & 0 \\ 0 & -\frac{1}{C_o} \end{bmatrix}$$

C. Combined system non-linear model

Fig.4 shows the non-linear model for the SPRC combining the state-space linear models of the ac and dc sub-systems. The mathematical square-root function represents the action the rectifier in Fig.2 linking the peak parallel capacitor voltage v_{Cp} to rectifier output voltage v_{Br}. If this non-linear mathematical relation is omitted, the entire large signal converter model becomes linear.

D. Linearization using state feedback scheme

The objective of the linearization scheme is to force either $v_{Cpd}=0$ or $v_{Cpq}=0$ to eliminate the mathematical non-linearity. This is obtained by orientation of the ac sub-system dq frame such that input voltages v_{ABd}` and $v_{ABq}$` are calculated accordingly to obtain $v_{Cpd}=v_c$ (the control variable) and $v_{Cpq}=0$. To obtain this, a state feedback measurement from output filter inductor current i_{Lo} is necessary. Fig. 5 shows how the state feedback scheme linearizes SPRC model. Coefficients k_1, k_3, k_5 and k_7 are circuit parameter dependent. Detailed in-depth analysis and derivation is given by the authors in [21].

E. Reduced order model

After linearizing the SPRC model, the resultant aggregate model is of eighth order due to combining both ac and dc sub-systems. This makes analysis and controller design a very cumbersome task. The state feedback linearization scheme ensures always that the two main conditions are satisfied

$$v_{Cpd} = v_c \quad \text{and} \quad v_{Cpq} = 0 \tag{3}$$

Therefore, the following relation is satisfied

$$\overline{v}_{Br} = \frac{2}{\pi}\sqrt{v_{Cpd}^{\ 2} + v_{Cpq}^{\ 2}} = \frac{2}{\pi}v_c \tag{4}$$

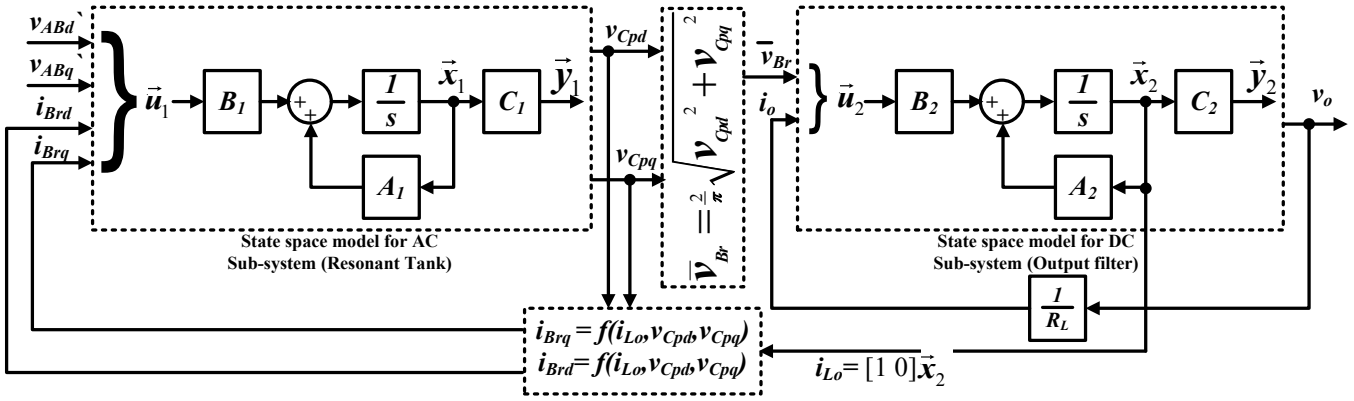


Fig. 4. Non-linear combined system model for the SPRC.

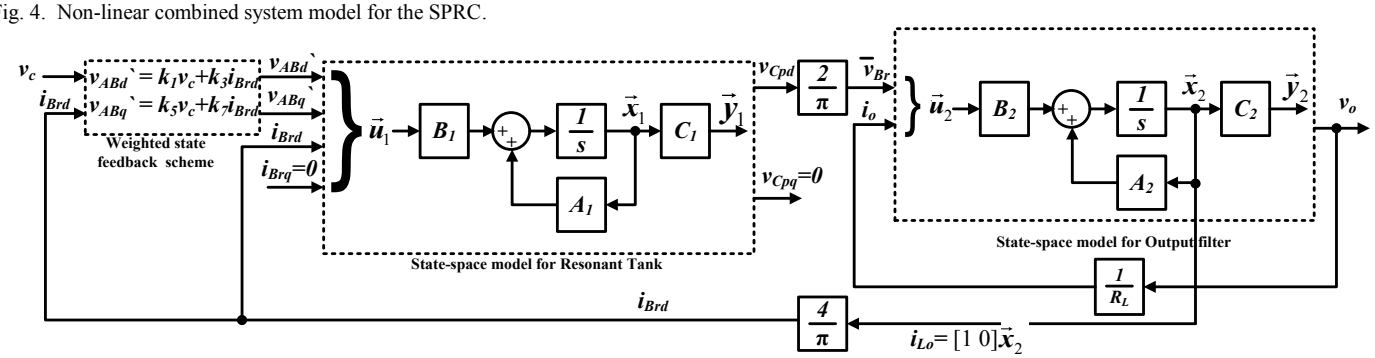


Fig. 5. Linearized model for the SPRC using weighted state feedback.

Consequently, control-to-output voltage transfer function can be approximated by the output filter circuit

$$\frac{v_o(s)}{v_c(s)} \approx \frac{2}{\pi}\frac{v_o(s)}{\bar{v}_{Br}(s)} \approx \frac{2}{\pi}\frac{1}{L_o C_o s^2 + r_{Lo} C_o s + 1} \tag{5}$$

This reduces the eighth order system model to a second order model, thanks to the slow output filter dynamics which dominate converter output voltage response compared to the fast resonant tank dynamics.

III. PREDICTIVE CONTROLLER DESIGN

Predictive control is a common control algorithm in applications such as active power filters, PWM rectifiers, current control of PWM inverters, ac drives, and distributed generation systems. Its application in the discrete time domain makes it suitable for DSP implementation. Predictive control of the phase-controlled SPRC has not been previously investigated. A two loop controller is designed with the outer loop performing output voltage regulation.

Since the reduced order SPRC model approximates the converter large signal model by the output filter (dc sub-system) model, therefore substituting (4) into (2) yields

$$\begin{aligned} \frac{di_{Lo}}{dt} &= \frac{1}{L_o}\left(-r_{Lo} i_{Lo} - v_o + \frac{2}{\pi} v_c\right) \\ \frac{dv_o}{dt} &= \frac{1}{C_o}(i_{Lo} - i_o) = \frac{1}{C_o}\left(i_{Lo} - \frac{1}{R_L} v_o\right) \end{aligned} \tag{6}$$

Discretizing (6) yields

$$v_c(k) = \frac{\pi}{2}\left(r_{Lo} i_{Lo}(k) + \frac{L_o}{T_s}(i_{Lo}(k+1) - i_{Lo}(k)) + v_o(k)\right) \tag{7}$$

$$i_{Co}(k) = i_{Lo}(k) - i_o(k) = \frac{C_o}{T_s}(v_o(k+1) - v_o(k)) \tag{8}$$

where T_s is the sampling (switching) frequency. Considering (8) and replacing $v_o(k+1)$ for $v_o^*(k+1)$ and $i_{Co}(k)$ for $i_{Co}^*(k)$, the output voltage loop can be constructed as

$$i_{Co}^*(k) = k_1\left(v_o^*(k+1) - v_o(k)\right) \tag{9}$$

where k_1 is the voltage loop predictive gain designed to obtain fast and stable response. With a high switching frequency (40 kHz), change in load current $i_o(k)$ can be neglected compared to change in $i_{Lo}(k)$ and $i_{Co}(k)$, hence it is an acceptable approximation to state that

$$\begin{aligned} i_o(k) &= i_o(k+1) \\ i_{Lo}(k+1) - i_{Lo}(k) &= i_{Co}(k+1) - i_{Co}(k) \end{aligned} \tag{10}$$

Substituting for instant $(k+1)$ by k in (9) yields the modified outer voltage loop structure

$$i_{Co}^*(k+1) = k_1\left(v_o^*(k+2) - v_o(k+1)\right) \tag{11}$$

Equating $i_{Co}(k+1)$ to $i_{Co}^*(k+1)$ in equation (10) yields

$$i_{Co}^*(k+1) - i_{Co}(k) = i_{Lo}(k+1) - i_{Lo}(k) \tag{12}$$

Comparing (12) with (7) enables the construction of the inner current loop where the control input can be obtained

$$v_c(k) = k_2\left(i_{Co}^*(k+1) - i_{Co}(k)\right) + \frac{\pi}{2}\left(r_{Lo} i_{Lo}(k) + v_o(k)\right) \tag{13}$$

where k_2 is the inner current loop predictive gain. Equation (13) shows that $i_{Co}(k)$ has to be measured for inner current loop

functionality. However, this is not a necessity since i_{Co} is proportional to change in v_o. Output voltage $v_o(k)$ is measured and $v_o(k+1)$ is necessary for realisation of the outer voltage loop (11). The advanced sample $v_o(k+1)$ can be predicted using the second order Lagrange quadratic formula

$$v_O(k+1) = 3v_O(k) - 3v_O(k-1) + v_O(k-2) \tag{14}$$

The predicted sample in advance $v_o(k+1)$ can be used to calculate $i_{Co}(k)$

$$i_{Co}(k) = \frac{C_O}{T_S}\left(v_O(k+1) - v_O(k)\right) \tag{15}$$

Therefore, $i_{Co}(k)$ for the inner current loop can be calculated using (15), with no need to sense it. Fig. 6 shows a schematic of the closed loop structure using the proposed predictive controller.

IV. CLOSED LOOP STABILITY

Considering the block diagram in Fig. 6, the closed loop system transfer function in the discrete z-domain can be expressed as

$$\frac{V_O(z)}{V_O^*(z)} = \frac{\left(\frac{2}{\pi}k_1k_2{T_S}^2\right)z^2}{a_4z^4 + a_3z^3 + a_2z^2 + a_1z + a_0} \tag{16}$$

where $a_4 = L_oC_o$, $a_3 = -2L_oC_o$, $a_2 = L_oC_o + \frac{4}{\pi}k_2C_oT_S + \frac{6}{\pi}k_1k_2{T_S}^2$, $a_1 = -\left(\frac{6}{\pi}k_2C_oT_S + \frac{6}{\pi}k_1k_2{T_S}^2\right)$ and $a_0 = \left(\frac{2}{\pi}k_2C_oT_S + \frac{2}{\pi}k_1k_2{T_S}^2\right)$.

Re-arranging the characteristic equation in (16) to take the form

$$1 + k_1GH(z) = 0 \tag{17}$$

The root locus can be drawn using the open loop gain $GH(z)$

$$GH(z) = \frac{\frac{2}{\pi}k_2{T_S}^2\left(3z^2 - 3z + 1\right)}{(L_oC_o)z^4 - (2L_oC_o)z^3 + \left(L_oC_o + \frac{4}{\pi}k_2C_oT_S\right)z^2 - \left(\frac{6}{\pi}k_2C_oT_S\right)z + \frac{2}{\pi}k_2C_oT_S} \tag{18}$$

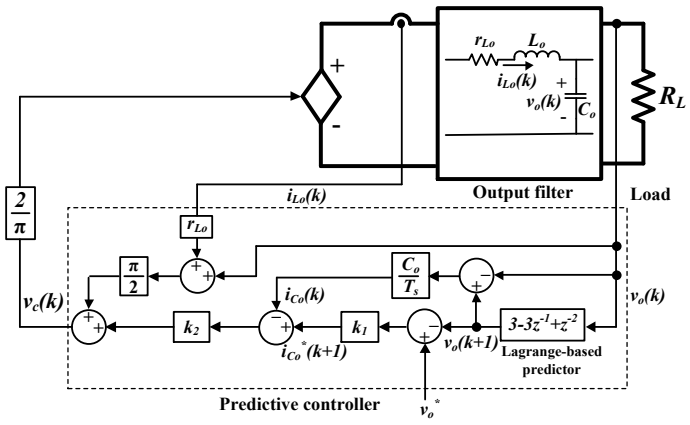


Fig. 6. Closed loop output voltage control using the proposed predictive controller

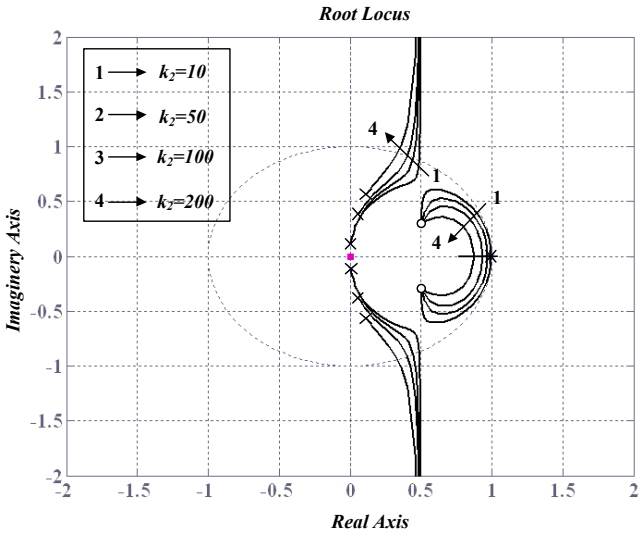


Fig.7. Root loci for system with proposed predictive controller.

In multi-loop control, the inner loop is faster than the outer loop; hence k_2 is selected to be greater than k_1. The outer loop is responsible for voltage regulation and overall closed loop stability. Therefore, for a given inner loop controller gain k_2, the system root locus can be plotted to study the stability limit of the closed loop with respect to change in k_1. Fig.7 shows the root loci for the closed loop system with circuit parameter values defined in Table I.

Fig. 7 shows that the closed loop system is more stable with smaller values of k_2. However, the inner loop dynamics are required to be faster, therefore the $k_1<k_2$ constrain would result in sluggish dynamic behaviour in the case of low k_2 gain; hence the trade-off between system speed of response and stability. In addition low gains generally result in poor controller disturbance rejection capability.

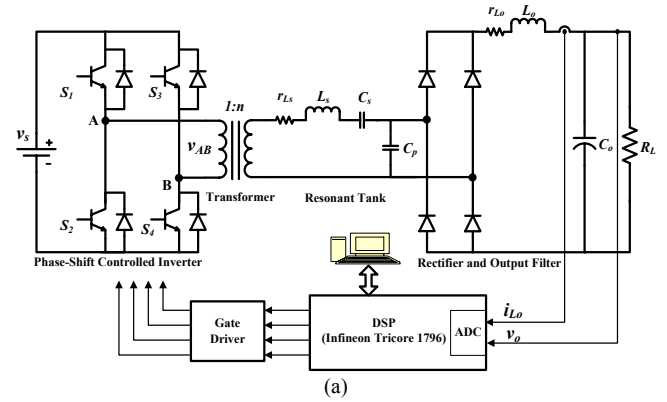
V. SIMULATION AND EXPERIMENTAL RESULTS

Fig. 8 shows the proposed predictive control algorithm implementation both experimentally and in simulation. Table I summarizes the circuit and control parameter values (k_1=0.24 and k_2=156). Measurements of the actual SPRC output voltage (v_o) and output filter inductor current (i_{Lo}) are taken; the former to perform voltage control and the latter for state feedback linearization as shown in Fig. 8(a) and (b). The state feedback scheme illustrated in Fig. 5 is implemented in Fig. 8(b). The phase shift angle δ between the inverter legs is then calculated by the algorithm in Fig. 8(c). All inverter switches are switched with a fixed 50% duty cycle; the only control variable being the phase shift angle δ between S_1 and S_3 as shown in Fig. 8(d). This controls the effective inverter output voltage duty cycle. The phase-shift angle is updated every switching cycle (25μs).

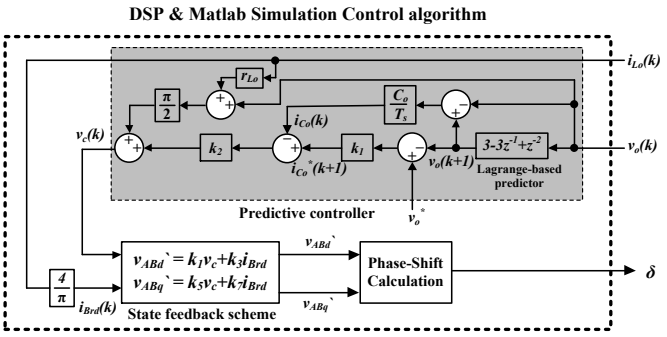
Fig. 9 shows simulation output voltage results comparing conventional PI control with the proposed predictive controller. Fig. 9(a) and (b) compare responses under step reference voltage (t=0) and step partial to full load ($R_{LPL}\rightarrow R_{LFL}$) applied at t=0.5s.

Table I
Resonant Converter Parameters

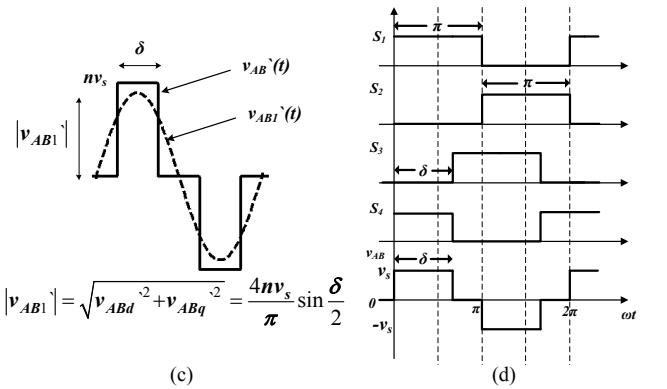
Parameter	*Value*
Internal resistance of resonant tank inductor r_{Ls}	0.1916 Ω
Resonant tank inductance L_s	100.13 µH
Parasitic transformer resistance referred to secondary r_l	0.6 Ω
Transformer Leakage inductance referred to secondary L_l	9.12 µH
Total equivalent resistance $r_T=r_l+r_{LS}$	0.7916 Ω
Total equivalent inductance $L_T=L_l+L_s$	109.25 µH
Resonant tank series capacitance C_s	0.255 µF
Resonant tank parallel capacitance C_p	0.255 µF
Internal resistance of output filter inductor r_{Lo}	0.5 Ω
Output filter inductance L_o	12.5 mH
Output filter capacitance C_o	120 µF
Resonant tank fundamental frequency f_s	40 kHz
Sampling period T_s	25µs
Supply voltage v_s	60V
Transformer turns ratio n	0.5
Full-load power rating of experimental test rig	40W
Part-load resistive load R_{LPL}	40.5 Ω
Full-load resistive load R_{LFL}	14.4 Ω
Reference output voltage v_o^*	24V



(a)



(b)



(c) (d)

Fig. 8. Closed loop structure (a) circuit diagram, (b) control algorithm, (c) phase-shift calculator, and (d) inverter phase control gating pattern.

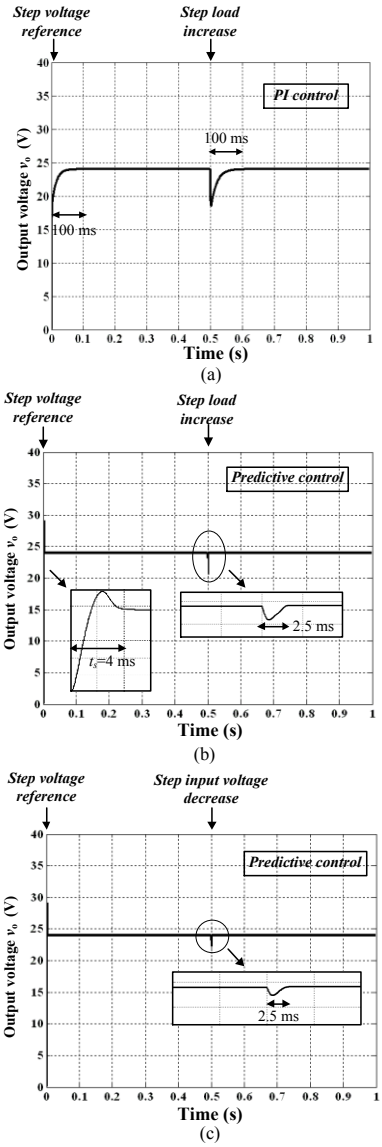
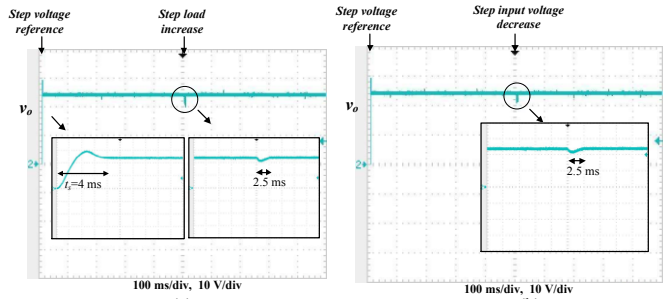


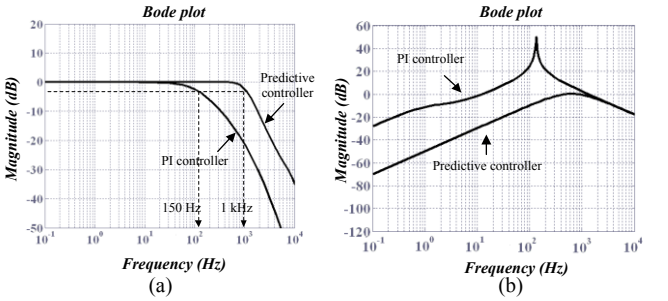
Fig. 9. Closed loop output voltage simulation results for (a) PI control with step load, (b) proposed predictive controller with step load, and (c) predictive control with step input voltage reduction.

Predictive controller response to step input voltage disturbance (v_s=60V to v_s=30V) applied at t=0.5s is illustrated in Fig. 9(c). The proposed predictive controller responds in a faster and robust manner to the applied disturbances compared to PI control. At startup, output voltage reaches desired reference value(v_o^*=24V) in 4ms compared to 100ms for PI control. This is due to the embedded feed forward mechanism that the controller implements which is represented by the ($v_o+r_{Lo}i_{Lo}$) term in (13) and which is also represented in Fig. 8(b). Existence of feed forward leads to stabilization of controller response enabling the use of high loop gains to speed up response and increase disturbance rejection capability. Improved robustness and disturbance rejection are apparent from Fig. 9(b) and (c). It takes the predictive controller 2.5ms to restore output voltage to reference value after application of both step load and step input voltage disturbances compared to 100ms for PI control. Voltage dip is higher with PI control.



(a) (b)

Fig. 10. Closed loop output voltage experimental results for proposed predictive controller (a) with step load disturbance, and (b) with step input voltage reduction.



(a) (b)

Fig. 11. Bode plots comparing the proposed predictive controller with PI control (a) closed loop bandwidth and (b) closed loop output impedance.

Fig. 10 depicts experimental results for the proposed predictive controller under the same operational disturbances. Fig. 11(a) shows a closed loop bandwidth comparison for the PI and proposed predictive controllers. The bandwidth of the predictive controller is 1 kHz compared to 150 Hz for the PI controller; hence the fast controller dynamic response. Fig. 11(b) shows the closed loop output impedance. The proposed controller has greater disturbance rejection capability, due to the higher attenuating nature of the closed loop output impedance compared to PI control.

VI. CONCLUSION

This paper proposed a new predictive output voltage controller for the phase-controlled SPRC. Controller design is based on a linearized converter large signal model utilising state feedback from output filter inductor current. Closed loop stability was studied and controller gains were selected to ensure stable response. Experimental and simulation results validated the enhanced closed loop output voltage response using the proposed controller in contrast with PI control. Faster dynamics and better robustness are achieved; thanks to the stabilizing feed forward path implemented by the predictive controller; hereby enabling the use of high loop gains.

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